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23494 7590 07/27/2005

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Robin E. Barnum (Depositor's name)
Robin E. Barnum (Signature)
August 9, 2005 (Date)

08/10/2005 TBESHAH2 00000032 200668 09713446

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/713,446	11/15/2000	VENKAT V EASWAR	TI-22423	3256

TITLE OF INVENTION: MULTI-LEVEL DITHER SCREENING ON A SPLIT ARITHMETIC LOGIC UNIT PROCESSOR

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1400	\$0	\$1400	10/27/2005
EXAMINER	ART UNIT	CLASS-SUBCLASS			
POON, KING Y	2624	358-003130			

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

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- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
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- 1 Robert D. Marshall, Jr.
2 W. James Brady, III
3 Frederick J. Telecky, Jr.

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(A) NAME OF ASSIGNEE

Texas Instruments Incorporated

(B) RESIDENCE: (CITY AND STATE OR COUNTRY)

Dallas, TX USA

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Authorized Signature Robert D. Marshall, Jr.
Typed or printed name Robert D. Marsahll, Jr.

Date August 9, 2005
Registration No. 28,527

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

TI-22423

Venkat V. Easwar

Art Unit: 2624

Serial No.: 09/713,446

Examiner: King Y. Poon

Filed: November 15, 2000

Conf. No.: 3256

For: Multi-Level Dither Screening on a Split Arithmetic Logic Unit Processor

CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that the following papers are being transmitted by facsimile to the U.S. Patent and Trademark Office at 703-746-4000 on the date shown below:


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August 9, 2005
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NAME OF INVENTOR(S): Venkat V. Easwar	
RECEIPT DATE & SERIAL NO.: Serial No.: 09/713,446 Filing Date: November 15, 2000	
TITLE OF INVENTION: Multi-Level Dither Screening on a Split Arithmetic Logic Unit Processor	
TI FILE NO.: TI-22423	DEPOSIT ACCT. NO.: 20-0668
FAXED: 8/9/05 DUE: 10/27/05 ATTY/SEC'Y: RDM/reb	

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